

SEMICONDUCTOR DEVICE WITH IMPROVED DESIGN FREEDOM OF EXTERNAL
TERMINAL

BACKGROUND OF THE INVENTION

Field of the Invention

5 This invention relates to a semiconductor device, and more particularly to a semiconductor device in which the degree of design freedom of an external terminal is increased in accordance with further increases in the number of external terminals.

Description of Related Art

10 Demands have been made in recent years for further reductions in the size and thickness of packaged semiconductor devices. In response to such demands, a packaging form known as a Wafer Level Chip Size Package (to be referred to simply as WCSP hereinafter), in which the external size of the packaging
15 is substantially equal to the external size of the semiconductor chip, has been proposed.

 A WCSP comprises a semiconductor chip. The semiconductor chip comprises a circuit element having a predetermined function and a plurality of electrode pads electrically connected to each
20 other on the circuit element. An insulating film is formed on the surface of the semiconductor chip such that the plurality of electrode pads is exposed.

 A plurality of wiring patterns connected to the exposed electrode pads is formed on the surface of the insulating film.

25 Electrode posts are formed on these wiring patterns. A sealing portion is then formed so as to cover the insulating film and wiring patterns and such that the top surface of the

electrode posts is exposed.

A plurality of external terminals provided as solder balls used in BGA packaging, for example, is provided on the top surface of the electrode posts.

5 This type of WCSP has a so-called fan-in configuration in which the multiple external terminals are provided in a lattice formation, for example, in a region corresponding to a circuit-forming surface of the semiconductor chip.

As regards the mounting of the semiconductor chip
10 comprising the external terminals in a fan-in configuration onto a printed board, Japanese Patent Application Laid-Open Publication No. 2000-208556 discloses a semiconductor device having the aim of preventing the breakage of a connecting portion between the printed board and external electrodes and comprising
15 a semiconductor chip having electrode pads, wiring which is formed in a predetermined position on the semiconductor chip and connected to the electrode pads, external electrodes which are formed in a predetermined position on the wiring and connected to the wiring, a printed board connected to the external
20 electrodes, and a substrate which is formed on the semiconductor chip. A resin layer is provided on the substrate for aligning the thermal expansion of the substrate and printed board, and in particular the external electrodes are provided on the resin layer.

25 As semiconductor devices become increasingly sophisticated, the number of external terminals formed on a single packaged semiconductor device is gradually increasing.

Conventionally, such demands for increases in the number of external terminals have been met by providing constitutions in which the spacing between adjacent external terminals is narrowed. As shall be described below, however, design freedom
5 is severely restricted by the disposal pitch and disposal positions of external terminals.

In the conventional WCSP described above, the minimum gap between adjacent external terminals is set at a concrete level of approximately 0.5mm. In the case of a 7mm×7mm WCSP, the number
10 of external terminals provided is approximately 160.

In accordance with demands for further increases in the number of external terminals on a packaged semiconductor device, it is desirable that approximately 300 external terminals be provided on a 7mm×7mm WCSP.

15 It is not technically impossible in the aforementioned WCSP to form an even larger number of external terminals on the surface of the WCSP by further narrowing the gap between adjacent external terminals.

However, it is extremely difficult to form 300 external
20 terminals on the surface area of a 7mm×7mm WCSP. Moreover, if the intervals between the external terminals are narrowed, an extremely high degree of technology is required to mount the WCSP onto a mounting substrate.

For example, the intervals between the plurality of
25 external terminals may have to be formed in alignment with the mounting pitch of the mounting substrate within a range of approximately 0.3mm to 0.7mm.

In a conventional packaging constitution in such a case, a semiconductor chip is connected to the substrate by means of a so-called flip chip connection and the semiconductor chip is connected to the external electrodes via the substrate.

5 Alternatively, the substrate and semiconductor chip are connected by wire bonding and the semiconductor chip is connected to the external electrode via the substrate. Since both of these connection methods utilize a substrate, and since additional sealing material is required in accordance with the height of
10 the wire loop, the package becomes thick. Moreover, the package becomes expensive due to the cost of the substrate. The package becomes particularly expensive when a flip chip connection is used since an expensive buildup substrate is required.

When connection is performed by means of wire bonding,
15 the inductance of the wire part increases.

An object of this invention is therefore to provide a semiconductor device having a constitution in which design freedom in the disposal pitch and disposal positions of external terminals is increased and the package itself can be made compact.

20 SUMMARY OF THE INVENTION

In order to achieve this object, a semiconductor device of this invention has the following constitution. That is, the semiconductor device of this invention comprises a semiconductor chip having a first main surface on which a plurality of electrode
25 pads is provided, a second main surface which opposes the first main surface, and one, two, or more side surfaces positioned between the first main surface and second main surface.

This semiconductor chip is surrounded by an extension portion which comprises a first surface and a second surface opposing the first surface and which is formed in contact with the side surfaces of the semiconductor chip such that the first surface is at a substantially equal level to the level of the first main surface.

An insulating film is formed on the first surface and first main surface such that each of the plurality of electrode pads, respectively is exposed.

Each of a plurality of wiring patterns is individually electrically connected to each of the electrode pads. These wiring patterns are extended from the electrode pads to the upper side of the first surface of the extension portion.

A sealing portion is formed on the insulating film on which the wiring patterns are formed such that a part of the wiring patterns is exposed.

A plurality of external terminals is provided in a region including the upper side of the extension portion so as to be electrically connected to the wiring patterns.

According to the constitution of the semiconductor device of this invention, external terminals can also be provided on the upper side of the extension portion which is provided in contact with and surrounding the semiconductor chip, and thus a semiconductor device having increased design freedom in the disposal pitch, disposal positions, and so on of the external electrodes can be provided. Further, the semiconductor device of this invention may be constructed without the use of an

interposer such as a substrate by applying a so-called WCSP manufacturing process, as a result of which increases in operating speed, functional sophistication, number of functions, and compactness can be achieved in comparison with a wire bonding connection. Moreover, an identical electrical characteristic can be obtained at a lower cost than a device in which a flip chip connection is used.

The manufacturing process for implementing this invention preferably comprises the following manufacturing steps.

A manufacturing method of the semiconductor device comprises the steps of:

(1) setting a plurality of semiconductor chip disposal regions on which a plurality of semiconductor chips is to be disposed at predetermined intervals on a lower base;

(2) providing a semiconductor chip having a first main surface on which a plurality of electrode pads are provided, a second main surface which opposes the first main surface, and a plurality of side surfaces positioned between the first main surface and second main surface on the semiconductor chip disposal region such that the second main surface faces the semiconductor chip disposal region;

(3) forming an extension portion having a first surface and a second surface which opposes the first surface on the lower base so as to contact the side surfaces of the semiconductor chip and thereby surround the semiconductor chip, and such that the level of the first surface is substantially equal to the level of the first main surface;

(4) forming an insulating film on the first surface of the extension portion and the first main surface such that a part of each of the electrode pads is exposed;

5 (5) forming a plurality of wiring patterns on the insulating film so as to be electrically connected to each of the electrode pads, respectively and extended from the electrode pads to the upper side of the first surface of the extension portion;

10 (6) forming a sealing portion on the wiring patterns and insulating film such that a part of each of the wiring patterns positioned on the upper side of the first surface is exposed;

15 (7) forming a plurality of external terminals over the wiring patterns in a region including the upper side of the extension portion and connecting the external terminals to the wiring patterns; and

(8) forming individual semiconductor devices comprising the semiconductor chip by cutting the extension portion between the plurality of semiconductor chips.

20 The manufacturing method of the semiconductor device also comprises the steps of:

(1) setting a plurality of semiconductor chip disposal regions on which a plurality of semiconductor chips is to be disposed at predetermined intervals on a lower base;

25 (2) providing a semiconductor chip having a first main surface on which a plurality of electrode pads are provided, a second main surface which opposes the first main surface, and a plurality of side surfaces positioned between the first main

surface and second main surface on the semiconductor chip disposal region such that the second main surface surfaces the semiconductor chip disposal region;

(3) forming an extension portion having a first surface and a second surface which opposes the first surface on the lower base so as to contact the side surfaces of the semiconductor chip and thereby surround the semiconductor chip, and such that the level of the first surface is substantially equal to the level of the first main surface;

(4) forming an insulating film on the first surface of the extension portion and the first main surface such that a part of the electrode pads is exposed;

(5) forming a plurality of wiring patterns on the insulating film so as to be electrically connected to each of the electrode pads and extended from the electrode pads to the upper side of the first surface of the extension portion;

(6) forming a plurality of electrode posts on each of the part of the wiring patterns positioned on the upper side of the extension portion;

(7) forming a sealing portion on the wiring patterns and insulating film such that the top surface of the electrode posts is exposed;

(8) forming external terminals on the top surface of the exposed electrode posts; and

(9) forming individual semiconductor devices comprising the semiconductor chip by cutting between the plurality of semiconductor chips.

The manufacturing method of the semiconductor device preferably further comprises a step of removing the lower base from the second surface of the extension portion and the second main surface following the step of forming the external
5 terminals.

The manufacturing method of the semiconductor device further comprises the steps of:

(1) preparing a jig comprising a plurality of concave portions;

10 (2) disposing a semiconductor chip having a first main surface on which a plurality of electrode pads are provided, a second main surface which opposes the first main surface, and a plurality of side surfaces positioned between the first main surface and second main surface within the concave portion such
15 that the second main surface faces the concave portion;

(3) forming an extension portion having a first surface and a second surface which opposes the first surface on the jig so as to contact the side surfaces of the semiconductor chip and thereby surround the semiconductor chip, and such that the
20 level of the first surface is substantially equal to the level of the first main surface;

(4) forming an insulating film on the first surface of the extension portion and the first main surface such that a part of each of the electrode pads is exposed;

25 (5) forming a plurality of wiring patterns on the insulating film so as to be electrically connected to each of the electrode pads, respectively and extended from the electrode

pads to the upper side of the first surface of the extension portion;

(6) forming a sealing portion on the wiring patterns and insulating film such that a part of each of the wiring patterns positioned on the upper side of the first surface is exposed;

(7) forming a plurality of external terminals over the wiring patterns in a region including the upper side of the extension portion and connecting the external terminals to the wiring patterns; and

(8) forming individual semiconductor devices comprising the semiconductor chip by cutting between the plurality of semiconductor chips.

The manufacturing method of the semiconductor device further comprises the steps of:

(1) preparing a jig comprising a plurality of concave portions;

(2) disposing a semiconductor chip having a first main surface on which a plurality of electrode pads are provided and a plurality of side surfaces positioned between the first main surface and a second main surface within the concave portion such that the second main surface faces the concave portion;

(3) forming an extension portion having a first surface and a second surface which opposes the first surface on the jig so as to contact the side surfaces of the semiconductor chip and thereby surround the semiconductor chip, and such that a part of each of the level of the first surface is substantially equal to the level of the first main surface;

(4) forming an insulating film on the first surface of the extension portion and the first main surface such that the electrode pads are exposed;

5 (5) forming a plurality of wiring patterns on the insulating film so as to be electrically connected to each of the electrode pads, respectively and extended from the electrode pads to the upper side of the first surface of the extension portion;

10 (6) forming electrode posts which are electrically connected to each of the part of the wiring patterns positioned on the upper side of the extension portion;

(7) forming a sealing portion over the wiring patterns and insulating film such that the top surface of the electrode posts is exposed;

15 (8) forming external terminals on the top surface of the exposed electrode posts;

(9) removing the jig from the second surface of the extension portion and the second main surface; and

(10) forming individual semiconductor devices
20 comprising the semiconductor chip by cutting between the plurality of semiconductor chips.

The manufacturing method of the semiconductor device preferably further comprises a step of, following the aforementioned step (2), suction-holding the semiconductor chip
25 on a bottom surface portion of the concave portion by means of a through hole provided in the concave portion and a suction and exhaust system connected to the through hole. The step of

forming the insulating film on the first surface of the extension portion and the first main surface such that a part of the electrode pads is exposed is preferably performed following this suction-holding step.

5 According to this manufacturing method for the semiconductor device of this invention, a semiconductor device with increased functional sophistication, number of functions, and compactness can be provided by means of a comparatively easy process. In particular, design freedom in the disposal pitch,
10 disposal positions, and so on of the external electrodes can be greatly increased.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features and advantageous of the present invention will be better understood
15 from the following description taken in connection with the accompanying drawings, in which:

Fig. 1(A) is a plan view seen from above showing in outline the constitution of a semiconductor device of this invention, and Fig. 1(B) is a plan view showing an expanded outline of the
20 main parts of a region of Fig. 1(A) in order to illustrate the connection relationship between a wiring pattern and electrode pads;

Figs. 2(A) and 2(B) are schematic sectional views showing cross sections severed along a broken line I-I in Fig. 1(A),
25 Fig. 2(A) showing an aspect in which a lower base is provided, and Fig. 2(B) showing an aspect in which the lower base is not provided;

Figs. 3(A) and 3(B) are a schematic plan view seen from above and a sectional view for illustrating a first manufacturing method for the semiconductor device of this invention;

5 Figs. 4(A) and 4(B) are a schematic plan view seen from above and a sectional view proceeding from Fig. 3 for illustrating the first manufacturing method for the semiconductor device of this invention;

10 Figs. 5(A) and 5(B) are a schematic plan view seen from above and a sectional view proceeding from Fig. 4 for illustrating the first manufacturing method for the semiconductor device of this invention;

15 Fig. 6(A) is a schematic plan view seen from above for illustrating the first manufacturing method for the semiconductor device of this invention, and Fig. 6(B) is a sectional view severed along a broken line I-I in Fig. 6(A);

Fig. 7 is a sectional view corresponding to Fig. 6;

20 Figs. 8(A) and 8(B) are a schematic plan view seen from above and a sectional view proceeding from Figs. 6 and 7 for illustrating the first manufacturing method for the semiconductor device of this invention;

Figs. 9(A) and 9(B) are a schematic plan view seen from above and a sectional view proceeding from Fig. 8 for illustrating the first manufacturing method for the semiconductor device of this invention;

25 Figs. 10(A) and 10(B) are a schematic plan view seen from above and a sectional view proceeding from Fig. 9 for illustrating the first manufacturing method for the semiconductor device of

this invention;

Fig. 11 is a schematic plan view and a sectional view (1) of a jig which is preferably used in a manufacturing method for the semiconductor device of this invention;

5 Fig. 12 is a schematic sectional view (2) of the jig which is preferably used in a manufacturing method for the semiconductor device of this invention;

Fig. 13 is a schematic sectional view (1) for illustrating a second manufacturing method for the semiconductor device of
10 this invention; and

Fig. 14 is a schematic sectional view (2) proceeding from Fig. 13 for illustrating the second manufacturing method for the semiconductor device of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

15 An embodiment of this invention will be described below with reference to the drawings. Note that in the drawings, the form, magnitude, and positional relationships of each constitutional component are merely illustrated schematically in order to facilitate understanding of this invention and no
20 particular limitations are placed on this invention thereby. Further, although specific materials, conditions, numerical value conditions, and so on are used in the following description, these are merely one preferred example thereof and therefore do not place any limitations on this invention. It is to be
25 understood that similar constitutional components in the drawings used in the following description are allocated and illustrated with identical reference symbols, and that duplicate

description thereof has occasionally been omitted.

A semiconductor device according to this invention will be described with reference to Figs. 1 and 2. Fig. 1(A) is a plan view seen from above showing in outline the constitution of a semiconductor device, and Fig. 1(B) is a plan view showing an expanded outline of the main parts of the region of Fig. 1(A) which is surrounded by a solid line 11 in order to illustrate the connection relationship between a wiring pattern and electrode posts. Figs. 2(A) and 2(B) are schematic sectional views showing cross sections severed along a broken line I-I in Fig. 1(A). Note that Fig. 2(A) shows a constitutional example in which the semiconductor device 10 of this invention is provided with a lower base 12 on its bottom surface side. Fig. 2(B) shows a constitutional example in which the lower base 12 is not provided.

The semiconductor device 10 of this invention comprises a semiconductor chip 30 on a lower base 12. The semiconductor chip 30 comprises a first main surface 36, a second main surface 38 which opposes the first main surface 36, and one, two, or more side surfaces 37 positioned between the first main surface 36 and second main surface 38. The semiconductor chip 30 further comprises a circuit element having a predetermined function and a plurality of electrode pads 34 electrically connected to the circuit element. The plurality of electrode pads 34 is provided on the first main surface 36. The plurality of electrode pads 34 is formed around the peripheral edge of the first main surface 36.

The semiconductor chip 30 is provided on the lower base 12 such that the first main surface 36 becomes the upper surface, or in other words such that the second main surface 38 faces a semiconductor chip disposal region 14.

5 The semiconductor device 10 of this invention comprises an extension portion 20 on the lower base 12. The extension portion 20 is provided on the side surfaces 37 of the semiconductor chip 30 disposed in the semiconductor chip disposal region 14 on the lower base 12, or in other words contacting the surfaces
10 of the semiconductor chip 30 other than the first and second main surfaces to thereby surround the semiconductor chip 30. This extension portion 20 is formed such that the level (i.e. height, as below) of a first surface 20a thereof is substantially equal to the level of the first main surface 36 of the
15 semiconductor chip 30.

The extension portion 20 may be appropriately selected from an organic material such as epoxy resin or silicone resin, for example. That is, a so-called liquid resin or mold resin may be applied.

20 In order to prevent warping of the semiconductor device 10 of this invention during the manufacturing process, the extension portion 20 is preferably formed from a material having a larger molding shrinkage than the molding shrinkage of a subsequently formed sealing portion.

25 Here, "molding shrinkage" indicates shrinkage of a single material occurring during a molding process. In other words, "molding shrinkage" corresponds to the sum of curing shrinkage

at molding temperature and thermal contraction occurring during the return from molding temperature to normal temperature.

More specifically, the extension portion 20 is preferably formed from a liquid resin having a coefficient of linear expansion within a lower temperature range than glass transition point of less than $1.5 \times 10^{-5}/^{\circ}\text{C}$ and a modulus of elasticity within a range of 7.8 to 22 GPa. A case in which mold resin is applied to the extension portion 20 will be described hereinafter.

An insulating film 40 is formed on the first surface 20a of the extension portion 20 and the first main surface 36 such that a part of each of the plurality of electrode pads 34 is exposed.

A plurality of wiring patterns 42 is formed on the surface of the insulating film 40 so as to be electrically connected to the exposed electrode pads 34, respectively.

A sealing portion 44 is provided on the respective surface regions of the semiconductor chip 30 and extension portion 20 so as to cover the wiring patterns 42 and insulating film 40. The insulating film 40 and sealing portion 44 described above are also referred to collectively as an insulating layer 48. Electrode posts 46 are provided so as to pass from each of the wiring patterns 42 through the sealing portion 44 to reach the surface of the sealing portion 44. A part of the electrode posts 46 is provided on the upper side of (directly above) the semiconductor chip 30, and the remaining electrode posts 46 are provided on the upper side of (directly above) the extension portion 20. These electrode posts 46 are normally arranged at

a constant pitch. The top surface of each electrode post 46 is exposed on the surface of the sealing portion 44. The electrode posts 46 are also referred to as post electrodes, and external terminals 47 are provided on the exposed top surface thereof. Solder balls 47a are usually provided as the external terminals 47. These external terminals 47 are provided at a wider pitch than the arrangement pitch of the electrode pads 34.

Here, using Fig. 1(B), the connection relationships between the electrode pads 34 and wiring patterns 42 will be described. A partial region (the region surrounded by the solid line) 11 of Fig. 1(A) has been expanded and illustrated in order to facilitate understanding of these connection relationships. The wiring patterns 42 are constituted such that each of the electrode posts (shown as 46 in Fig. 2) connected to the lower portion of the external terminals 47 is regularly and electrically connected to a corresponding electrode pad 34. A long wire 42a, a medium wire 42b, and a short wire 42c, for example, are provided as the wires which constitute each wiring pattern 42. These wires 42a, 42b, and 42c are respectively connected in that order to the corresponding electrode pad 34 in a one-on-one connection relationship of one wire to one electrode pad.

The wiring patterns 42 are provided in a region on the upper side of (directly above) the semiconductor chip 30 and on the upper side of (directly above) the extension portion 20, or in other words so as to straddle the boundary of an extended region 21. More specifically, at least a part of the plurality

of wiring patterns 42 is individually electrically connected to each of the electrode pads 34 such that the electrode pads 34 are extended from the upper side of the first main surface to the upper side of the first surface 20a of the extension portion 20 discretely insulated from one another.

Hence the portions 42X of the wiring patterns 42 having a certain length on or in the vicinity of this boundary is preferably comprised of thicker and/or wider wire.

In other words, portions of the wiring patterns on a boundary and vicinity thereof between semiconductor chip and the extension portion are formed wider or more thickly than other portions of said wiring patterns.

By forming the partial region 42X of the wiring patterns 42 at which stress is considered more likely, due to such phenomena as thermal stress and particularly an edge effect, to be thicker in this manner, operational reliability in the semiconductor device 10 is improved.

The region on the upper side of (directly above) the extension portion 20 is referred to as the extended region 21 due to the fact that the external terminal forming region extends beyond the surface region of the semiconductor element. In this constitutional example, electrode posts 46 are also formed on the extended region 21.

The sealing portion 44 is formed so as to cover the wiring patterns 42 and electrode posts 46. The sealing portion 44 is formed such that a part of each of the electrode posts 46 is exposed.

The external terminals 47 are formed via the electrode posts 46. A constitution is also possible in which the external terminals are directly connected to the wiring patterns 42 without passing through the electrode posts by exposing a part of the wiring patterns 42 through the sealing portion 44.

In this constitutional example, the external terminals 47 are formed from solder balls 47a, for example. These solder balls 47a are provided on the top surface of the exposed electrode posts 46 and connected to the wiring patterns 42 via the electrode posts 46. The arrangement and pitch of adjacent electrode posts 46 may be set as desired in consideration of mounting onto a printed board or the like, for example.

As described above, the electrode posts 46 are provided not only within a surface area range corresponding to the upper side of the semiconductor chip 30, but also on the upper side of the extension portion 20, or in other words on the extended region 21. As a result, design freedom in the disposal positions and disposal pitch of the electrode posts 46 is increased. In other words, restrictions on the disposal pitch of the external terminals 47 are eased such that mounting is facilitated, and thus the electrode posts 46 can be formed at wider intervals and in a desired number in accordance with the constitutional requirements on the mounting substrate side, for example. More specifically, external terminals can be formed at a desired disposal pitch and in a desired number by appropriately adjusting the surface area of the formed extension portion 20.

By removing the lower base 12 as desired by peeling the

lower base 12 away in a manufacturing process to be described below, a thinner semiconductor device 10 such as that shown in Fig. 2(B) can be obtained.

According to the constitution of the semiconductor device 5 10 of this invention, the external terminals 47 are provided on the side surfaces 37 of the semiconductor chip 30, or in other words on the upper side of (directly above) the extension portion 20, that is the extended region 21, which is provided in contact with and so as to surround the surfaces of the semiconductor 10 chip 30 other than the first main surface 36 and second main surface 38. Thus the semiconductor device 10 can be constituted in a so-called fan-out constitution or a fan-in/fan-out constitution in which the external terminals 47 are also formed on the upper side of the first main surface 36. As a result, 15 design freedom in the disposal pitch, disposal positions, and so on of the external terminals 47 can be increased.

The semiconductor device 10 of this invention is constituted using a so-called WCSP manufacturing process such that the semiconductor chip 30 and external terminals 47 are 20 directly connected without the use of an interposer such as a substrate, and thus in addition to the aforementioned effect, the operational speed, functional sophistication, number of functions, and compactness of the semiconductor device 10 can be increased in comparison with a device in which a wire bonding connection, for example, is used. The semiconductor device 10 25 can also be obtained with an identical electrical characteristic to and at a lower cost than a device in which a flip chip connection,

for example, is used.

Next, a first manufacturing method for the semiconductor device of the first embodiment will be described with reference to Figs. 3(A) to 10(B).

5 As a rule, each Fig. (A) is a partial schematic plan view seen from above for illustrating the constitution of the semiconductor device of this invention, and each Fig. (B) is a schematic sectional view showing a cross section severed along a broken line I-I of the corresponding Fig. (A). To facilitate
10 description, Fig. 6(B) is an exception to this rule, being a partial enlarged view of the part of Fig. 6(A) which is surrounded by a solid line 11. Moreover, Fig. 7 is a schematic sectional view severed along the I-I line of Fig. 6(A).

First, a semiconductor chip disposal region 14 on which
15 the semiconductor chip 30 is to be placed is set on the prepared lower base 12. The profile of the semiconductor chip disposal region 14 substantially matches the profile of the semiconductor chip 30. The intervals between adjacent semiconductor chip disposal regions 14 are set to be equal. This interval is
20 preferably set to a sufficient value in consideration of the surface area of the margin required when the semiconductor devices are divided into individual units in a subsequent process, the surface area of the surface region of the extension portion which is formed in accordance with the desired number of external
25 terminals, and so on.

First, as shown in Figs. 3(A) and (B), position alignment between the set semiconductor chip disposal region 14 and the

lower base 12 is performed, whereupon the semiconductor chip 30 is disposed on the lower base 12.

As described above, the semiconductor chip 30 comprises a first main surface 36. The first main surface 36 is provided with the electrode pads 34. The electrode pads 34 are provided in a plurality around the peripheral edge of the semiconductor chip 30. The semiconductor chip 30 also comprises the second main surface 38 which opposes the first main surface 36 and one, two, or more side surfaces 37 positioned between the first main surface and second main surface.

Here, the lower base 12 may be formed from a plate-form or sheet-form body made of an organic material such as a glass epoxy or a polyimide, for example. Alternatively, the lower base 12 may be appropriately selected as desired from a ceramic substrate, a metallic substrate, an Si substrate, or similar. The surface of the lower base 12, or at least the region on which the semiconductor chip 30 is disposed, is preferably constituted by a member which is constituted by adhesion means (not shown) such as an adhesive.

The semiconductor chip 30 is preferably held on the semiconductor chip disposal region 14 by adhesion using the adhesion means.

Particularly if the semiconductor device of this invention is to be formed without a lower base as shown in Fig. 2(B), a lower base which can be easily removed in a subsequent step using a method such as peeling, for example, should be selected. Specifically, a thermal release sheet "Revalpha" (product name),

manufactured by Nitto Denko Corporation, heat-resistant "Icros Tape" (product name) or the "SP Series" (product name), manufactured by Mitsui Chemicals Inc., or similar may be applied as a lower base which can be peeled away at a later stage. A
5 glass substrate or the like on whose surface an ultraviolet curable adhesive, for example, is painted to serve as adhesion means may also be favorably applied.

Next, as shown in Figs. 4 (A) and (B), the extension portion 20 is formed on the side surfaces 37 of the semiconductor chip
10 30, or in other words in contact with and surrounding the surfaces of the semiconductor chip 30 other than the first and second main surfaces 36 and 38, so as to fill the gaps between the plurality of semiconductor chips 30.

As described above, the extension portion 20 may be applied
15 using a so-called liquid resin or mold resin as the material therefor. This material may be appropriately selected from an organic material such as epoxy resin or silicone resin, for example.

In order to prevent warping of the semiconductor device
20 10 during the manufacturing process, the extension portion 20 is preferably formed from a material having a larger molding shrinkage than the molding shrinkage of a subsequently formed sealing portion. More specifically, the extension portion 20 is preferably formed using as a material a liquid resin having
25 a coefficient of linear expansion at a lower temperature than the glass transition temperature of less than $1.5 \times 10^{-5}/^{\circ}\text{C}$ and a modulus of elasticity within a range of 7.8 to 22 GPa.

The following methods, for example, may be applied to the formation of the extension portion 20. (1) and (2) are methods employed when a liquid resin is applied to the extension portion 20, and (3) is a method employed when a mold resin is applied to the extension portion 20.

(1) Liquid resin is supplied by a dispensing method so as to fill the gaps between the plurality of semiconductor chips 30, whereupon the liquid resin is cured using appropriate curing means.

(2) Liquid resin is supplied by a precision printing method so as to fill the gaps between the plurality of semiconductor chips 30, whereupon the liquid resin is cured using appropriate curing means.

(3) The first main surface 36 of the semiconductor chip 30 is set in a die so as to be protected and mold resin is supplied by a transfer mold method so as to fill the gaps between the plurality of semiconductor chips 30. The mold resin is then cured using appropriate curing means.

Here, the height of the first surface 20a of the extension portion 20, that is a thickness d_2 , and the height of the first main surface 36 of the semiconductor chip 30, that is a thickness d_1 , preferably match. However, a slight height difference, undulation, or the like may exist as long as this difference is within the range of a difference of elevation at which the subsequently formed wiring patterns may be formed without the danger of the wires becoming disconnected or the like.

Dimensional accuracy in the direction of thickness may

be improved particularly when mold resin is applied to the extension portion 20, as a result of which the extension portion 20 may be formed with a higher degree of precision.

5 Next, the insulating film 40 is formed on the surface of the extension portion 20 and the first main surface 36. The insulating film 40 is formed such that the electrode pads 34 on the semiconductor chip 30 are at least partially exposed.

10 Here, a process may be used in which the insulating film 40 is formed to cover the electrode pads 34, whereupon the electrode pads 34 are exposed using a photolithography method or the like, for example.

15 As described above, a height difference may sometimes occur between the surface of the extension portion 20 and the surface of the semiconductor chip 30. An undulation or depression may also sometimes occur on the surface of the extension portion 20. In such cases, the insulating material for the insulating film 40 may be used to reduce this height difference such that wiring patterns can be formed in a subsequent step or to make the insulating film 40 substantially even.

20 Formation of the insulating film 40 may be performed using an appropriate insulating material and by means of a method which is suited to the material of the extension portion 20, for example a well-known method such as spin coating, printing, or direct application.

25 Next, as shown in Figs. 6 and 7, a plurality of wiring patterns 42 is formed on the surface of the insulating film 40. Formation of these wiring patterns 42 is performed following

setting such that each wiring pattern 42 is electrically connected to a corresponding electrode pad 34 on the surface of the insulating film 40 and in consideration of the disposal of the external terminals to be formed at a later stage.

5 More specifically, the wire width, wire spacing, optimum angles, and so on are determined in accordance with applicable wiring process rules such that connections can be made at the shortest possible distances. As shown in the drawings, for example, a plurality of wiring pattern groups, each comprising
10 a long wire 42a, a medium wire 42b, and a short wire 42c, is formed in respect of the plurality of electrode pads 34 formed around the peripheral edge of the semiconductor chip 30 at the shortest possible distances, and one end portion of each wire is connected to the corresponding electrode pad 34. An electrode
15 post mounting pad is formed on the other end portion so that an external terminal 47 (solder ball 47a) can be connected thereto via an electrode post. In other words, each of the plurality of wiring patterns 42 is individually electrically connected to each of the electrode pads 34 on the insulating film 40 such
20 that the electrode pads 34 are extended from the upper side of the first main surface 36 to the upper side of the first surface 20a of the extension portion 20.

 Note that to facilitate description, the disposed electrode pads 34 in Figs. 5(A) and 6(A) are illustrated
25 schematically in a smaller number than the actual number.

 The wiring patterns 42 may be formed by performing a wiring pattern formation process in a well-known WCSP manufacturing

process such as sputtering or photolithography on the upper side of the extension portion 20 on the surface region of the insulating film 40, or in other words a desired region on the insulating film 40 including the extended region 21. The material used to form the wiring patterns 42 may be selected appropriately at will, but is preferably a material such as aluminum, copper, or a metal alloy. The wiring patterns 42 may be formed by selecting an appropriate material such as copper, for example.

Next, as shown in Figs. 8 (A) and 8 (B), the electrode posts 46 are formed on the surface of each wiring pattern 42 so as to be electrically connected thereto. The electrode posts 46 are provided in the extended region 21 on the upper side of (directly above) the extension portion 20 and in the region near the extended region 21 on the upper side of (directly above) the semiconductor chip 30. The electrode posts 46 are formed in a lattice formation and arranged at predetermined intervals. As described above, these intervals may be set in consideration of mounting, or in other words as either constant or irregular intervals.

After an appropriate material has been selected, the electrode posts 46 may be formed by means of an electrode post 46 forming process in a well-known WCSP manufacturing process such as plating or photolithography.

The sealing portion 44 is formed so as to cover the surface of the insulating film 40 on which the wiring patterns 42 and electrode posts 46 are formed. The sealing portion 44 is formed such that a part of the extended parts of the wiring patterns

42 (or the wiring patterns 42 themselves when electrode posts are not formed) is exposed.

This sealing process may be implemented by means of a well-known method using a well-known sealing material such as an epoxy mold resin.

A mold resin generally used here has the following property values, for example: a linear expansion coefficient at a lower temperature than glass transition temperature within a range of 0.6 to $1.3 \times 10^{-5}/^{\circ}\text{C}$; a glass transition temperature (T_g) within a range of 125 to 220°C ; and a modulus of elasticity within a range of 9.8 to 24 GPa (1000 to 2450 kg/mm^2). These values may be favorably applied to the semiconductor device 10 of this invention.

As described above, and particularly when the extension portion 20 is formed from a so-called mold resin similarly to the sealing portion 44, the material is determined such that the molding shrinkage of the mold resin used to form the extension portion 20 is larger than that of the sealing portion 44 in order to prevent warping of the semiconductor device 10 during the manufacturing process. The following combinations can be cited as examples of the properties of the mold resin used for the extension portion 20 and sealing portion 44.

(1) Extension portion/sealing portion: the properties of the extension portion mold resin are a linear expansion coefficient at a lower temperature than glass transition temperature within a range of 1.1 to $1.5 \times 10^{-5}/^{\circ}\text{C}$ and a glass transition temperature (T_g) which is larger than 170°C ; the

properties of the sealing portion mold resin are a linear expansion coefficient at a lower temperature than glass transition temperature of less than $1.0 \times 10^{-5}/^{\circ}\text{C}$, a glass transition temperature (T_g) within a range of 125 to 220°C , and a modulus of elasticity within a range of 14.7 to 24 GPa (1500 to 2450kg/mm^2).

(2) Extension portion/sealing portion: the properties of the extension portion mold resin are a linear expansion coefficient at a lower temperature than glass transition temperature within a range of 1.1 to $1.7 \times 10^{-5}/^{\circ}\text{C}$, a glass transition temperature (T_g) which is lower than 170°C , and a modulus of elasticity within a range of 9.8 to 19.6 GPa (1000 to 2000kg/mm^2); the properties of the sealing portion mold resin are a linear expansion coefficient at a lower temperature than glass transition temperature of less than $1.0 \times 10^{-5}/^{\circ}\text{C}$, a glass transition temperature (T_g) within a range of 125 to 220°C , and a modulus of elasticity within a range of 14.7 to 24 GPa (1500 to 2450kg/mm^2).

(3) Extension portion/sealing portion: the properties of the extension portion mold resin are a linear expansion coefficient at a lower temperature than glass transition temperature within a range of 1.1 to $1.7 \times 10^{-5}/^{\circ}\text{C}$, a modulus of elasticity of 13.7 GPa (1400kg/mm^2), and a glass transition temperature (T_g) within a range of 125 to 170°C ; the properties of the sealing portion mold resin are a linear expansion coefficient at a lower temperature than glass transition temperature of less than $1.0 \times 10^{-5}/^{\circ}\text{C}$, a glass transition

temperature (T_g) within a range of 125 to 220°C, and a modulus of elasticity within a range of 14.7 to 24 GPa (1500 to 2450 kg/mm²).

Next, as shown in Figs. 9(A) and 9(B), the surface side of the sealing portion 44 is trimmed such that the top surface (also referred to as the upper surface) of the electrode posts 46 is trimmed and exposed.

This process may be performed using a well-known grinding or polishing process.

A method such as film formation may also be applied to the formation of the sealing portion 44. In this case, substantially no load is placed on the electrode posts 46. Also in this case, the sealing portion 44 can be formed such that the top surface of the electrode posts 46 is directly exposed on the surface of the sealing portion 44 without the need for a grinding process on the sealing portion 44 as described above.

At this time, any suitable processing required from a design point of view may be performed on the exposed top surface of the electrode posts 46. If copper is used as the material for the electrode posts 46, for example, an Ni (nickel) film or the like may be formed on the top surface of the electrode posts 46 as a barrier metal layer.

The plurality of external terminals 47 is formed on the wiring patterns 42 in the region including the upper side of the extension portion 20 to be individually electrically connected to the extended part of the wiring patterns 42, or in other words the exposed part thereof.

In this constitutional example, solder balls 47a, for

example, are formed as the external terminals 47 on the upper surface of the electrode posts 46 which is exposed through the surface of the sealing portion 44.

Next, as shown in Figs. 10(A) and 10(B), the extension portions 20 and sealing portion 44 between the plurality of semiconductor chips 30 are severed along a cutting line shown in the drawings by a dot/dash line a to provide individual constitutional bodies comprising a single semiconductor device having a predetermined function.

This singularization process is preferably performed using a blade or the like which rotates at high speed, for example.

Next, as desired, the lower base 12 is removed from the second surface 20b of the extension portion 20 and the second main surface 38 of each divided constitutional body by being peeled away therefrom.

When the lower base 12 is constituted by peelable adhesion means such as those described above or peelable adhesion means are provided on the lower base 12 in the manufacturing process, the lower base 12 should be peeled away using processing corresponding to the adhesion means such as heating, processing using heated water, or ultraviolet radiation. More specifically, when a thermal release sheet is applied as the lower base 12, for example, the lower base 12 may be peeled away by heating the adhesion means to a predetermined temperature. If ultraviolet curable adhesive is applied as the adhesion means, for example, the lower base 12 may be removed by curing the adhesive using ultraviolet radiation.

This peeling process may be executed either following the electrode post 46 forming step, the sealing step, or the singularization step. Considering the mechanical strength and so on of the extension portion 20, however, peeling is preferably performed at the end of the sealing step.

In the description of the manufacturing method for the semiconductor device of this invention, an example was illustrated in each of the drawings in which a plurality of semiconductor devices 10 is manufactured simultaneously by disposing a plurality of semiconductor chips in a 2 (vertical) \times X (horizontal, X being a positive number of no less than 2) lattice formation on the lower base or jig. However, this invention is not limited thereto, and semiconductor devices may be manufactured simultaneously by arranging a larger number of semiconductor chips in a larger lattice formation.

Since a WCSP manufacturing process can be applied to the first manufacturing method, the semiconductor device 10 can be manufactured without the need for any special manufacturing processes for the semiconductor device 10.

Next, a second manufacturing method for the semiconductor device of this invention will be described with reference to Figs. 11(A) through 14(C). Note that in the following manufacturing processes, the applied materials, process implementation conditions, and so on are similar to those in the first method and hence detailed description thereof has been omitted.

The second manufacturing method differs in that the jig

50 is used to implement each process in place of the lower base 12 described in the first manufacturing method.

First the constitution of a preferred jig to be applied to the second manufacturing method will be described with reference to Figs. 11 and 12.

Fig. 11(A) is a partial schematic plan view illustrating the constitution of a preferred jig to be applied to the second manufacturing method of the semiconductor device of this invention, and Fig. 11(B) is a schematic sectional view showing a cross section severed along the I-I broken line in Fig. 11(A).

Fig. 12 is a schematic sectional view for illustrating the constitution of a modified example of the jig in Fig. 11 which is preferably applied to the second manufacturing method of this invention. Note that in Fig. 12, the plan view seen from above is similar to Fig. 11(A), and hence illustration and detailed description thereof have been omitted.

The jig 50 is a tool used in the manufacturing process for supporting or aligning constitutional elements. In this constitutional example, the jig 50 is a pedestal comprising a plurality of concave portions 52 at equal intervals and in a lattice formation. The interval between adjacent concave portions 52 is preferably determined in consideration of the surface area of the extension portion required for the semiconductor device 10 to be manufactured, or in other words the disposal positions, disposal pitch, disposal number, and so on of the external electrodes.

In this example, the concave portions 52 of the jig 50

are set as depressions in rectangular parallelepiped form. There are no particular limitations on this form, however, as long as semiconductor chips 30 having various forms can be held by the concave portions 52 with stability and do not interfere with the implementation of subsequent processes.

A depth h of each concave portion 52 and the surface area of a bottom surface portion 52a should be set sufficiently to allow the semiconductor chips 30 to be held by and fixed on the jig 50 with stability and to allow the implementation of subsequent processes.

When the first and second main surfaces 36 and 38 of the semiconductor chip 30 are rectangular parallelepipeds with identical form and size, for example, the surface area of the bottom surface portion 52a of the concave portion 52 is preferably set to be equal to the surface area of at least the second main surface 38, and such that side wall portions 52b of the concave portion 52 are perpendicular to the bottom surface portion 52a.

Alternatively, as shown in Fig. 12, the surface area of the bottom surface portion 52a of the concave portion 52 (including the surface area of a through hole 56 to be described hereinafter) may be set smaller than the surface area of the second main surface 38 and such that the side wall portions 52b of the concave portion 52 are inclined, whereby the distal end thereof becomes gradually thinner toward the interior of the concave portion 52.

In this case, as shown by the dotted line in Fig. 12, the semiconductor chip 30 is held by the jig 50 within the inclined

region of the side wall portions 52b such that the jig 50 contacts a region in the vicinity of the edges of the semiconductor chip 30 on the second main surface 38 side, or in other words the periphery of and the vicinity of the periphery of the second
5 main surface 38. By means of this constitution, the region of the semiconductor chip 30 which contacts the jig 50 is minimized, and thus the step of removing the semiconductor chip 30 from the jig 50 becomes extremely easy.

Further, since the semiconductor chip 30 may be supported
10 within the range of the incline of the side wall portions 52b, a plurality of semiconductor chips 30 having various different sizes may be used with one type of jig.

The jig 50 is preferably constituted by a material such as a metal or ceramic which has a low adhesiveness in respect
15 of the semiconductor chip 30 or an appropriate material coated with Teflon (registered trademark) or the like which has a low adhesiveness in respect thereof. In so doing, the step of peeling an unfinished constitutional body including the semiconductor device away from the jig 50 may be implemented easily.

20 A through hole 56 is preferably formed in the concave portion 52 of the jig 50. A suction and exhaust system 58 for suction-holding the semiconductor chip 30 in the concave portion 52 is preferably connected to the through hole 56.

The suction and exhaust system 58 may be constituted by
25 a well-known evacuation system comprising a vacuum pump, piping, and so on, for example.

Next, the second manufacturing method using the jig 50

for the semiconductor device of this invention will be described with reference to Figs. 13(A) through 14(C).

In Figs. 13 and 14, the plan views seen from above are similar to those of the first manufacturing method and hence illustration and description thereof have been omitted. The second manufacturing method will therefore be described with reference to the schematic sectional views.

First, the jig 50 is prepared as described above with reference to Figs. 11 and 12.

Then, as shown in Fig. 13(A), the semiconductor chip 30 is set inside the concave portion 52 such that the second main surface 38 of the semiconductor chip 30 faces the bottom surface 52a of the concave portion 52 of the jig 50. If the surface area of the bottom surface portion 52a of the concave portion 52 is set smaller than the surface area of the second main surface 38 and the side wall portions 52b defining the periphery of the concave portion 52 are inclined toward the interior of the concave portion 52 as shown in Fig. 12, the semiconductor chip 30 is provided on the jig 50 within the inclined region of the side wall portions 52b such that the jig 50 contacts the region in the vicinity of the edges of the semiconductor chip 30 on the second main surface 38 side, or in other words the periphery of and the vicinity of the periphery of the second main surface 38.

If the through hole 56 and the suction and exhaust system 58 which is connected thereto are provided in the bottom surface portion 52a of the concave portion 52 in the jig 50 as described

above, air is preferably evacuated thereby from the contact surface (gap) between the second main surface 38 of the semiconductor chip 30 and the bottom surface portion 52a of the concave portion 52 such that the semiconductor chip 30 is suction-held on the jig 50.

The degree of evacuation required for suction-holding the semiconductor chip 30 on the jig 50 should be sufficient to enable the semiconductor chip 30 to be held with stability.

Next, as shown in Fig. 13(B), the extension portion 20 is formed on the surfaces of the semiconductor chip 30 other than the first and second main surfaces 36 and 38, or in other words in contact with and surrounding the side surfaces 37 of the semiconductor chip 30.

The extension portion 20 is formed such that the level of the first surface 20a thereof is substantially equal to the level of the first main surface 36 of the semiconductor chip 30.

Formation of the extension portion 20 is performed by making a selection from the methods and materials described above. If the side wall portions 52b of the jig 50 are inclined as described above, a slight gap (space) may occur between the jig 50 and the lower portion of the side surface portion of the semiconductor chip 30. Although no further processing is required for this gap if the gap is within a range which does not interfere with subsequent processes, in particular formation of the wiring patterns, the extension portion 20 may be formed as desired such that the gap does not occur.

Next, the insulating film 40 is formed on the surface of the extension portion 20 and first main surface 36 of the semiconductor chip 30 which are formed on the jig 50 such that the electrode pads 34 provided on the semiconductor chip 30 are exposed.

Next, as shown in Fig. 13(C), the plurality of wiring patterns 42 is formed on the surface of the insulating film 40 so as to be electrically connected to the top surface of the respective electrode pads 34. In this case, similarly to the first manufacturing method, the wiring patterns 42 and electrode pads 34 are connected in a one-on-one relationship of one wiring pattern to one electrode pad.

Then, as shown in Fig. 14(A), one electrode post 46 is formed on and connected to each wiring pattern 42. The electrode posts 46 are provided in the extended region 21 on the upper side of (directly above) the extension portion 20 and in the region on the upper side of (directly above) the semiconductor chip 30 in the vicinity of the extended region 21.

Next, the sealing portion 44 is formed covering the surface of the insulating film 40 on which the wiring patterns 42 and electrode posts 46 are formed.

Then, as shown in Fig. 14(B), the sealing portion 44 is trimmed from the surface side thereof such that the top surface of the electrode posts 46 is exposed.

The solder balls 47a serving as the external terminals 47 are then formed on the exposed top surface of the electrode posts 46.

Then, as shown in Fig. 14(C), the jig 50 is peeled away from the second surface 20b of the extension portion 20 and the second main surface 38 following release of the vacuum if vacuum suction means are employed.

5 The plurality of adjacent semiconductor chips 30 are then severed to form individual semiconductor devices 10 comprising the semiconductor chip 30.

By means of such a process, a semiconductor device is manufactured having a substantially identical constitution to
10 the semiconductor device manufactured according to the first manufacturing method described above.

Note that in the semiconductor device manufactured according to the second manufacturing method, step are produced by the concave portions 52 of the jig 50 on the bottom surface
15 side of the semiconductor device, or more specifically between the second surface 20b of the extension portion 20 and the second main surface 38 of the semiconductor chip 30. If not desired, however, no further processing is necessary.

According to the second manufacturing method, a single
20 jig can be used repeatedly. Since there is no need to use a lower base as in the first manufacturing method, the number of members required in the manufacturing process can be reduced. As a result, a reduction in manufacturing costs can be expected. Further, when the semiconductor chip is suction-held on the jig
25 by a suction and exhaust system via a through hole, holding the semiconductor chip on the jig and removing the semiconductor device therefrom can be performed easily and speedily such that

an increase in the throughput of the manufactured semiconductor devices can be expected.

In all embodiments of this invention, the electrode posts 46 are preferably formed from a conductive material. This material is preferably copper. A thin oxidation layer is preferably formed on the surface of the electrode posts 46 at this time. In so doing, the adhesive property between the electrodeposts 46 and the sealing portion 44 is improved, thereby improving resistance to moisture.

In all embodiments of this invention the solder balls 47a are formed on the electrode posts 46 as the external terminals 47. A so-called BGA (Ball Grid Array) has been described, but this invention is not limited thereto. For example, a so-called LGA (Land Grid Array) may be formed by applying and reflow soldering solder paste onto the exposed electrode posts 46 or implementing Ni/Au processing by means of electroless plating.

In all embodiments of this invention, the sealing portion may be formed not only in a so-called saw-cut form, but may also be formed not matching the profile of the lower base and/or the extension portion as long as the extent of this misalignment is within a range which does not impair the object of this invention.

The semiconductor device 10 according to the first embodiment described above may be constituted as a stacked body of a plurality of semiconductor devices 10. In this case, for example, through holes may be formed in the extension portion using a well-known method to thereby form stacking terminals.